Key Specifications

CPU
- Dual-core ARM Cortex A9 processor
- Independent I-cache, D-cache, and L2 cache
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor

3D GPU
- Quad-core high-performance GPU
- OpenGL ES 2.0/1.1/1.0 and OpenVG 1.1
- EGL

Memory Interfaces
- DDR3/3L SDRAM interface
  - Maximum 2 GB memory capacity
  - 32-bit wide memory
  - Maximum 800 MHz or 1600 MHz frequency
- SPI flash interface
  - 1-/2-/4-bit flash memory
  - Maximum 32 MB SPI flash capacity
- NAND flash interface
  - SLC/MLC flash memory
  - Toggle 1.0/2.0 or ONFI 2.0/3.0
  - 8-bit data width
  - Maximum 64 GB NAND flash capacity
  - Maximum 80-bit ECC
- eMMC flash interface

Video Decoding
- H.264 BP/MP/HP@ level 5.0; MVC
- MPEG1
- MPEG2 SP@ML and MP@HL
- MPEG4 SP@L0–3 and ASP@L0–5; GMC
- MPEG4 short header format (H.263 baseline)
- DivX 3/4/5/6
- AVS baseline @level 6.0 and AVS-P16
- RealVideo 8/9/10
- VC-1 SP@ML, MP@HL, and AP@L0-3
- VP6/VP8
- 1080p@60 fps decoding
- Low-delay decoding
- Simultaneous multi-channel decoding

Image Decoding
- Full HD JPEG hardware decoding, a maximum of 64 megapixels
- MPEG baseline decoding, a maximum of 1080p@40 fps decoding capability
- PNG hardware decoding, a maximum of 64 megapixels

Video and Image Encoding
- H.264 BP/MP/HP@level 4.2 video encoding, a maximum of 1080p@30 fps encoding capability
- JPEG hardware encoding, a maximum of 1080p@30 fps encoding capability
- CABAC
- VBR or CBR mode for video decoding
- Inter-frame prediction and intra-frame prediction
- Fast motion estimation algorithm
- Low-delay encoding
- Encoding of multiple ROIs

Audio Encoding and Decoding
- Dedicated audio DSP
- G.711(u/a) audio decoding
- MPEG L1/L2
- DRA and RealAudio decoding
- Dolby Digital and Dolby Digital Plus
- Dolby True HD and Dolby Digital Plus transcoding
- DTS and DTS HD core decoding
- DTS and Dolby Digital transparent transmission
- AAC-LC and HE AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- Down mixing and resampling
- 2-channel audio mixing and echo cancellation
- Intelligent volume control
- SRS, Dolby, and MS11 sound effects
- Pounding bass processing
- G.711(u/a), AMR-NB, AMR-WB, and AAC-LC encoding

TS Demultiplexing/PVR
- One embedded DVB-C QAM demodulator, compliant with J.83 A/B/C
- A maximum of four TS inputs and one IF input
- A maximum of two TS outputs
- QAM loopback output
- A maximum of 96 hardware PID channels
- Full-service PVR
- Recording of scrambled and non-scrambled streams

Security Processing
- Advanced security features
- DRM
- OTP
- AES, DES, and 3DES data encryption and decryption
- Hardware hash algorithm
- Content protection for USB devices
- Content protection for SATA or eSATA hard disk
- Downloadable CA

Graphics and Display Processing
- Hardware overlaying of multi-channel graphics and video inputs
- 5-layer OSD
- Four video layers
- A maximum of 2560 x 1600 picture output
- Mosaic and multi-region display
Hi3716C V200 Brief Data Sheet

- Mirroring display
- 16-bit or 32-bit color depth
- Image or video rotation
- Letterbox and pan and scan
- 3D video processing and display
- Multi-tap vertical and horizontal scaling of videos and graphics; free scaling
- Low-delay display
- Enhanced full-hardware TDE
- Full-hardware anti-aliasing and anti-flicker
- CSC with configurable coefficients
- Image enhancement and denoising
- Deinterlacing
- Sharpening
- Chrominance, luminance, contrast, and saturation adjustment
- Db/Dr processing for graphics and videos

Audio and Video Interfaces
- PAL, NTSC, and SECAM standard output, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9 and forcible aspect ratio conversion
- 1080p60/1080p50/1080p30/1080p24/1080i60/1080i50/720p/576i/480p/480i outputs
- One SD output and one HD output from the same source or different sources
- Two HD outputs from the same source or different sources
- Digital video interfaces
  - One HDMI 1.4a TX output interface with HDCP 1.2
  - One BT.656/601 or BT.1120 video input interface and extended HDMI 1.4a RX input interface
  - One BT.1120 video output interface
  - One LCD output interface
- Analog video interfaces
  - One CVBS interface
  - One YPbPr or VGA interface
  - Four embedded VDACs that integrate video buffers and support cable detection
- Configurable CVBS or YPbPr output for each VDAC
- Rovi and VBI
- Audio interfaces
  - Audio-left and audio-right channels
  - SPDIF interface
  - Embedded ADAC
  - Two I²S or PCM digital audio inputs/outputs
  - HDMI audio output

Peripheral Interfaces
- One SATA 3.0 host interface
- Three USB 2.0 host ports, one supporting the host/device function
- One 4-bit SDIO 3.0 interface with integrated LDO, supporting 3.3 V or 1.8 V components
- Two 10/100/1000 Mbit/s GE MACs with one integrated Fast Ethernet PHY
- Two smart card interfaces, supporting T0, T1, and T14 protocols
- One IR receiver with two input interfaces
- One LED and keypad control interface
- Four I²C interfaces
- Five UART interfaces
- Multiple GPIO interfaces
- Four PWM interfaces
- Integrated POR module

Others
- 2-layer PCB design
- Various boot modes
- Boot program download and execution over a serial port or USB port
- Integrated standby processor, supporting various low-power modes and less than 30 mW standby power consumption
- Low-power design such as AVS and DVFS
- 2.5 W typical working power consumption
- PBGA558 package with 23 mm x 23 mm (0.91 in. x 0.91 in.) body size and 0.8 mm (0.03 in.) pitch
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Hi3716C V200 Brief Data Sheet

Functional Block Diagram

With an integrated high-performance Cortex A9 dual-core processor and embedded NEON, Hi3716C V200 meets differentiated service requirements. To meet the growing requirements on multimedia playback, video communication, multi-screen transcoding, and multi-room applications, Hi3716C V200 supports HD video decoding in various formats, including MPEG2, H.264, AVS+, RealVideo8/9/10, VC-1 AP, VP6, and VP8, and high-performance H.264 HD encoding. Hi3716C V200 provides a smooth man-machine interface and rich gaming experience with a high-performance 2D/3D acceleration engine. It also enables flexible connection schemes with two GE ports, one integrated Ethernet PHY, three USB 2.0 ports, one independent SDIO 3.0 port, one SATA 3.0 port, and more peripheral interfaces. Hi3716C V200 complies with mainstream advanced security requirements.
Typical Application Block Diagram

- HDMI
- YPbPr/CVBS/VGA
- Line out
- SPDIF
- Microphone/Line in
- Camera
- LCD
- SPI flash
- NAND flash
- DDR3/DDR3L
- DC power/clock/reset
- LED/GPIO/Keypad
- IR receiver
- WiFi
- WiFi/SD
- UART
- USB 2.0
- SATA 3.0
- MII/RMII/RGMII
- BT.656/601/1120
- USB
- SDIO
- RS232
- USB 2.0 device
- HDD
- FE/GE PHY

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- RealVideo 8/9/10 and RealAudio, mentioned in this document, are intellectual property of RealNetworks, Inc. Any parties intending to use RealVideo 8/9/10 and RealAudio must obtain the appropriate license from RealNetworks, Inc.
## Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>ADAC</td>
<td>audio DAC</td>
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<tr>
<td>AES</td>
<td>advanced encryption standard</td>
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<tr>
<td>AVS</td>
<td>audio/video coding standard</td>
</tr>
<tr>
<td>AVS</td>
<td>adaptive voltage scaling</td>
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<tr>
<td>CABAC</td>
<td>context-based adaptive binary arithmetic coding</td>
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<tr>
<td>CBR</td>
<td>constant bit rate</td>
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<tr>
<td>CSC</td>
<td>color space conversion</td>
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<tr>
<td>CVBS</td>
<td>composite video broadcast signal</td>
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<tr>
<td>DES</td>
<td>data encryption standard</td>
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<tr>
<td>DRM</td>
<td>digital rights management</td>
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<tr>
<td>DSP</td>
<td>digital signal processor</td>
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<tr>
<td>DVFS</td>
<td>dynamic voltage and frequency scaling</td>
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<tr>
<td>GPIO</td>
<td>general purpose input/output</td>
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<tr>
<td>GPU</td>
<td>graphics processing unit</td>
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<tr>
<td>HDCP</td>
<td>high-bandwidth digital content protection</td>
</tr>
<tr>
<td>HDMI</td>
<td>high definition multimedia interface</td>
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<tr>
<td>I/O</td>
<td>input/output</td>
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<tr>
<td>I²C</td>
<td>inter-integrated circuit</td>
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<tr>
<td>I²S</td>
<td>inter-IC sound</td>
</tr>
<tr>
<td>IR</td>
<td>infrared</td>
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<tr>
<td>LCD</td>
<td>liquid crystal display</td>
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<tr>
<td>MLC</td>
<td>multi-level cell</td>
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<tr>
<td>OTP</td>
<td>one-time programmable</td>
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<tr>
<td>PBGA</td>
<td>plastic ball grid array</td>
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<tr>
<td>PCM</td>
<td>pulse code modulation</td>
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<tr>
<td>PID</td>
<td>packet ID</td>
</tr>
<tr>
<td>POR</td>
<td>power-on reset</td>
</tr>
<tr>
<td>PVR</td>
<td>personal video recorder</td>
</tr>
<tr>
<td>PWM</td>
<td>pulse width modulation</td>
</tr>
<tr>
<td>ROI</td>
<td>region of interest</td>
</tr>
<tr>
<td>SLC</td>
<td>single-level cell</td>
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<tr>
<td>SPDIF</td>
<td>Sony/Philips digital interface</td>
</tr>
<tr>
<td>UART</td>
<td>universal asynchronous receiver transmitter</td>
</tr>
<tr>
<td>VBR</td>
<td>variable bit rate</td>
</tr>
<tr>
<td>VDAC</td>
<td>video digital-to-analog converter</td>
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